CLAIMS

What is claimed is:

1. A circuit having scan circuitry comprising:

a) a constant power area that receives constant power;

b) a switched power area that receives interruptible power; and

c) an inactive state power reduction manager disposed in the constant power area for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state-save, and for asserting a power control signal that is used to disconnect the switched power area from a power supply pad; and for receiving a wake up signal, and responsive thereto for de-asserting the power control signal that is used to connect the switched power area to the power supply pad, for performing a scan-based state restore, and for de-asserting the stop clock signal to resume the normal mode clock.

2. The circuit of claim 1 further comprising:

d) a power switch coupled to the inactive state power reduction manager for receiving the power control signal and responsive thereto for selectively removing power from the switched power area.

3. The circuit of claim 2 wherein the power switch is a field effect transistor (FET) having a first electrode coupled to a power source, a second electrode coupled to the switched power area, and a third electrode for receiving the power control signal.

4. The circuit of claim 1 wherein the inactive state power reduction manager generates a plurality of scan control signals to perform the scan-based state store and scan-based state restore; and wherein the scan control signals includes a scan clock signal.

5. The circuit of claim 1 wherein the inactive state power reduction manager employs the scan circuitry to save state information and to restore state information.

6. The circuit of claim 1 wherein the wake-up signal is one of an internal wake-up signal and an external wake-up signal.

7. The circuit of claim 1 wherein the wake-up signal provided by one of a human trigger, an application, and a timer.

8. The circuit of claim 1 further comprising:

d) a memory for storing the state information; and

wherein the inactive state power reduction manager provides address signals and memory control signals to the memory and manages memory operations that read state information from and write state information to the memory.

9. The circuit of claim 8 wherein the memory is one of a volatile memory and a non-volatile memory.

10. The circuit of claim 9 wherein the volatile memory is a random access memory.

11. The circuit of claim 8 wherein the memory is disposed in one of the constant power area and the switched power area.

12. The circuit of claim 1 wherein the circuit is implemented in a board level application.

13. A method for inactive state power reduction for a circuit that has scan circuitry and a switched power portion comprising:

a) receiving a sleep signal;

responsive to the sleep signal,

b) stopping a normal mode clock;

c) performing a state save by employing the scan circuitry;

d) disconnecting the switched power portion of the circuit from power;

e) receiving a wake-up signal;

responsive to the wake-up signal,

f) re-connecting the switched power portion of the circuit to power;

g) performing a state restore by employing the scan circuitry; and

h) re-starting the normal mode clock.

14. The method of claim 13 wherein performing a state save using the scan circuitry includes

using the scan circuitry to obtain state information from the circuit; and

storing the state information in a memory.

15. The method of claim 14 wherein the step of storing the state information in a memory comprises the steps of:

performing a write operation on the memory to write the state information to the memory.

16. The method of claim 13 wherein performing a state restore using the scan circuitry includes

reading the previously stored state information from a memory; and

using the scan circuitry to write the state information to the circuit.

17. The method of claim 16 wherein the step of reading the previously stored state information from a memory comprises the steps of:

performing a read operation on the memory to access the state information.

18. A circuit board comprising:

a) a first integrated circuit having a test access port;

b) a second integrated circuit having a test access port; and

c) an inactive state power reduction manager coupled to the first integrated circuit and the second integrated circuit for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state save of state information of the first integrated circuit and the second integrated circuit, and for asserting a power control signal that is used to disconnect the first integrated circuit and the second integrated circuit from a power supply; and for receiving a wake up signal, and responsive thereto for de-asserting the power control signal that is used to re-connect the first integrated circuit and the second integrated circuit to the power supply, for performing a scan-based state restore for restoring state information to the first integrated circuit and the second integrated circuit, and for de-asserting the stop clock signal to resume the normal mode clock.

19. The circuit of claim 18 further comprising:

d) a power switch coupled to the inactive state power reduction manager for receiving the power control signal and responsive thereto for selectively removing power from the first integrated circuit and the second integrated circuit.

20. The circuit of claim 18 further comprising:

a memory for storing the state information; and

wherein the inactive state power reduction manager provides address signals and memory control signals to the memory and manages memory operations that read state information from and write state information to the memory.